

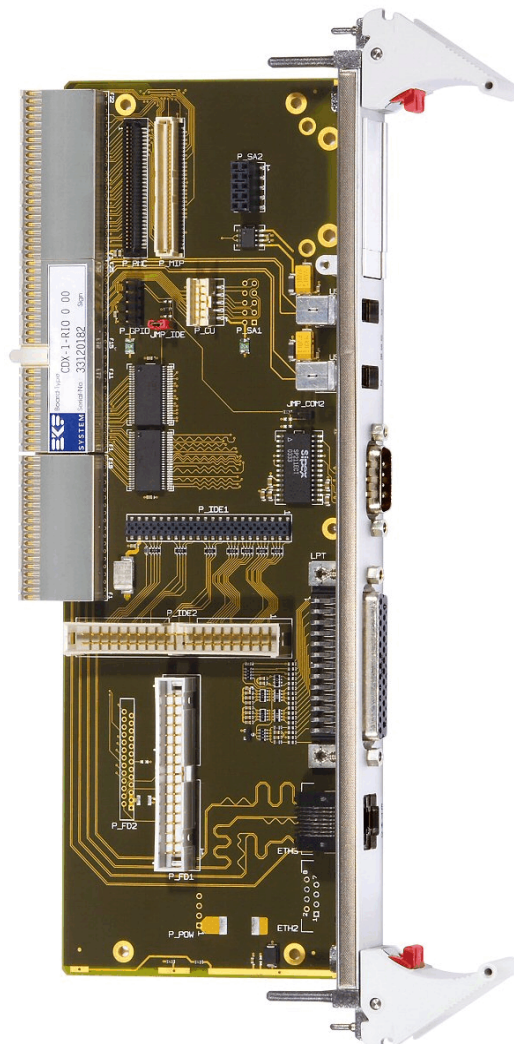


## Technical Information

### CDX-RIO • Rear I/O Transition Module

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## Contents

About this Manual . . . . .	3
Edition History . . . . .	3
Related Documents . . . . .	4
Nomenclature . . . . .	4
Trade Marks . . . . .	4
Legal Disclaimer - Liability Exclusion . . . . .	4
CDX-RIO Features . . . . .	5
Short Description . . . . .	6
Image CDX-RIO . . . . .	7
Image CDX-RIO w CD1-OPERA . . . . .	8
Block Diagram CDX-RIO . . . . .	9
Block Diagram C00-HD Option . . . . .	10
Top View Component Assembly . . . . .	11
On-Board Connectors . . . . .	12
Back Panel Connectors . . . . .	13
Installing and Replacing Components . . . . .	14
Before You Begin . . . . .	14
Warnings . . . . .	14
Caution . . . . .	14
Installing the Board . . . . .	15
Removing the Board . . . . .	16
EMC Recommendations . . . . .	17
Technical Reference . . . . .	18
Caution . . . . .	18
Back Panel Connectors . . . . .	19
ETH2 / ETH3 Ethernet . . . . .	20
COM2 Serial Port . . . . .	21
LPT Parallel Port . . . . .	22
USB2 / USB3 High Speed Serial Bus . . . . .	23
Mezzanine Bezel . . . . .	24
On-Board Connectors . . . . .	25
P-CU Serial Interface Connectors . . . . .	30
P-FD1 Floppy Disk Drive . . . . .	31
P-FD2 Floppy Disk Drive . . . . .	32
P-IDE1 IDE . . . . .	33
P-IDE2 IDE/ATA . . . . .	34
P-GPIO Connector . . . . .	35
P-MIP Mezzanine Connector . . . . .	36
P-PMC Mezzanine Connector . . . . .	37
Power Connector P-POW . . . . .	38
P-SA1 / P-SA2 Serial Interface Connectors . . . . .	39
Schematics . . . . .	40

## About this Manual

This manual is a short form description of the technical aspects of the CDX-RIO, required for installation and system integration. It is intended for the very advanced user only.

## Edition History

EKF Document	Ed.	Contents/ <i>Changes</i>	Author	Date
Text # 3223 cdx_tie.wpd	1	Technical Information CDX-RIO English Preliminary edition	jj	22. Sep 03
	2	Changed illustrations: Back panel, COM2, ETH2/3, LPT, USB2/3	jj	14 October 2003
	3	Added drawing 'Mezzanine Adapter Module'	jj	20 October 2003
	4	Added drawing 'Component Assembly'	jj	30 October 2003
	5	Added images CDX-RIO	jj	14 June 2004
	6	Mixed up designations P-IDE1 & P-IDE2 corrected	jj	29 September 2004

## Related Documents

- ▶ CD1-OPERA User Guide. For a description of the CD1-OPERA CPU card, which acts as a controller board with respect to the CDX-RIO transition module, please refer to the correspondent CPU user guide, available by download at [http://www.ekf.de/c/ccpu/cd1/cd1\\_e.html](http://www.ekf.de/c/ccpu/cd1/cd1_e.html).
- ▶ PICMG® 2.0 R3.0 CompactPCI Specification
- ▶ IEEE P1386.1 / Draft 2.4 PMC Mezzanine Cards
- ▶ VITA 29 Draft 0.94b PC•MIP Specification

## Nomenclature

Signal names used herein with an attached '#' designate active low lines.

## Trade Marks

Some terms used herein are property of their respective owners, e.g.

Pentium, Celeron: ® Intel, *CompactPCI*: ® PICMG, Windows 2000, Windows XP: ® Microsoft

EKF does not claim this list to be complete.

## Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

## CDX-RIO Features

Feature Summary	
Form Factor	80x233mm <sup>2</sup> , back panel width 4HP (20.3mm) w/o hard disk mezzanine module, 8HP (40.6mm) with hard disk option, height 6U
On-Board Connectors <sup>1</sup>	IDE/ATA 40-pin header 2.54mm, IDE/ATA 44-pin header 2.00mm, serial port header 2x5-position 2.00mm (TTL level, suitable for EKF CU series modules), serial port header 2x5-position 2.54mm (TTL level, suitable for MEN SA series modules), 34-pin floppy disk drive header 2.54mm, 26-position micro floppy disk connector 1mm ZIF FFC/FPC, GPIO port header 2x5 position 2.54mm, IEEE1386 mezzanine connector (PMC), IEEE1386 mezzanine connector (PC•MIP), +5V power connector
Back Panel Connectors <sup>1</sup>	ETH3 Ethernet (RJ45), COM2 RS-232E (9-pos. D-Sub male), LPT parallel printer port (25-pos. D-Sub female), USB2 & USB3 (type A connectors), bezel for mezzanine rear I/O adapter
CPCI Connectors <sup>1</sup>	Metric connectors 2.00mm, J3 5x19 (Ethernet option), J4 5x25, J5 5x22 (PMC/PC•MIP mezzanine option)

<sup>1</sup> Please note: The CDX-RIO is predominantly a custom specific product. Not all of the components mentioned in this manual may be present on your actual board. Please discuss your individual needs with sales@ekf.de before buying this component.

## Short Description

Available as a companion board to the CD1-OPERA CPU card, the CDX-RIO is provided with several additional I/O ports. Being mainly a passive rear I/O transition module, groups of signals from the CD1 CPU board are passed across the CompactPCI J3/P3, J4/P4 and J5/P5 connectors to the CDX transition module.

While the IDE and FD as well as other utility signals are available locally on the CDX for internal attachment of ATA devices and a floppy disk drive, other connectors like USB2/3 and ETH3 are mounted into the back panel for external use.

An optional add-on module to the CDX-RIO is provided with either one or two 2.5" IDE hard disk drives. This option requires an 8HP rear panel for the entire assembly, in contrast to the 4HP back panel of the CDX-RIO w/o hard disks.

Utilization of the CDX-RIO transition module adds a level of I/O functionality, which is not available with the CD1 CPU board alone. Further on, swapping the CPU card is simplified by means of rear I/O, which is important for efficient system maintenance (MTTR).

Image CDX-RIO

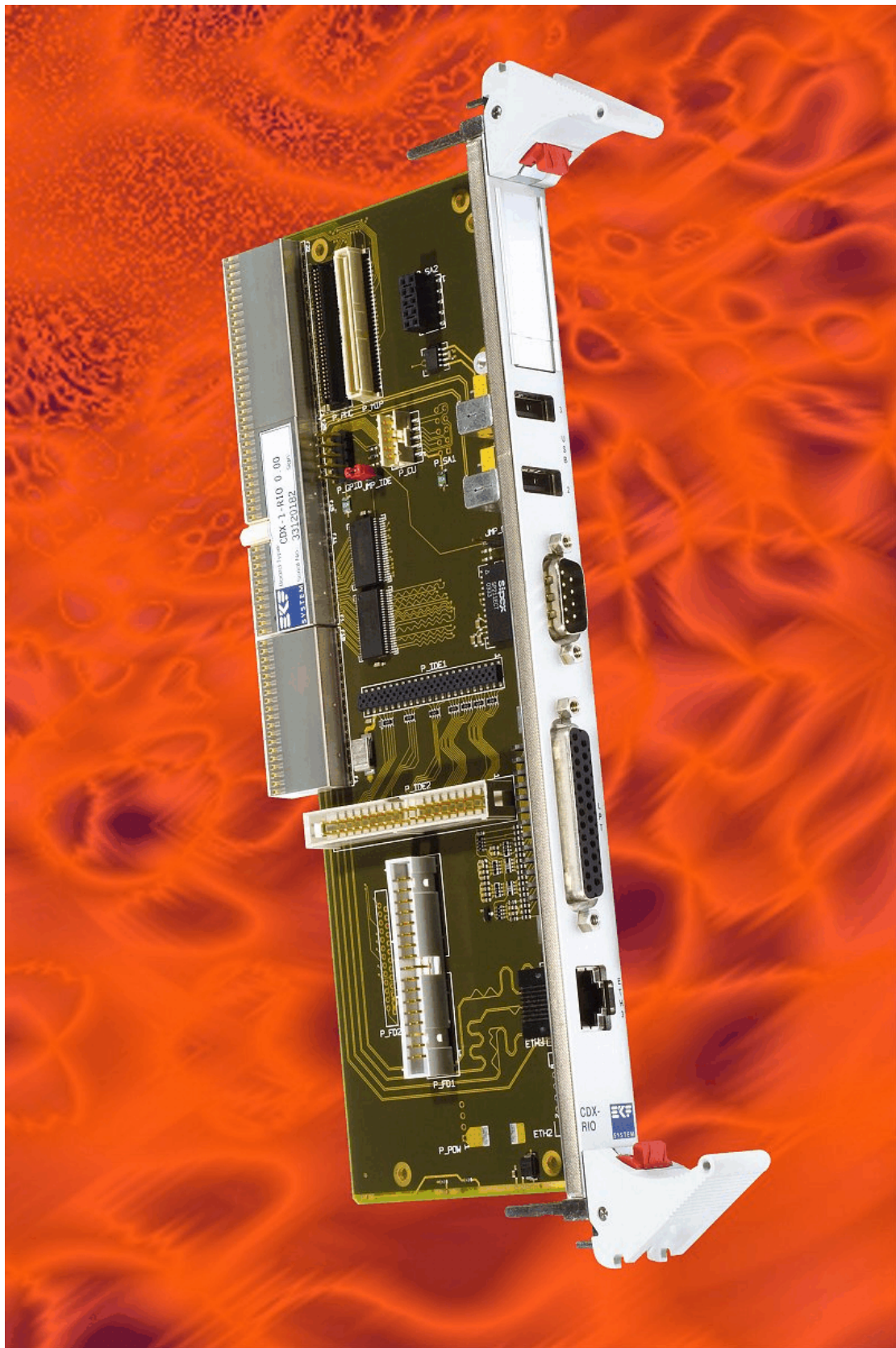
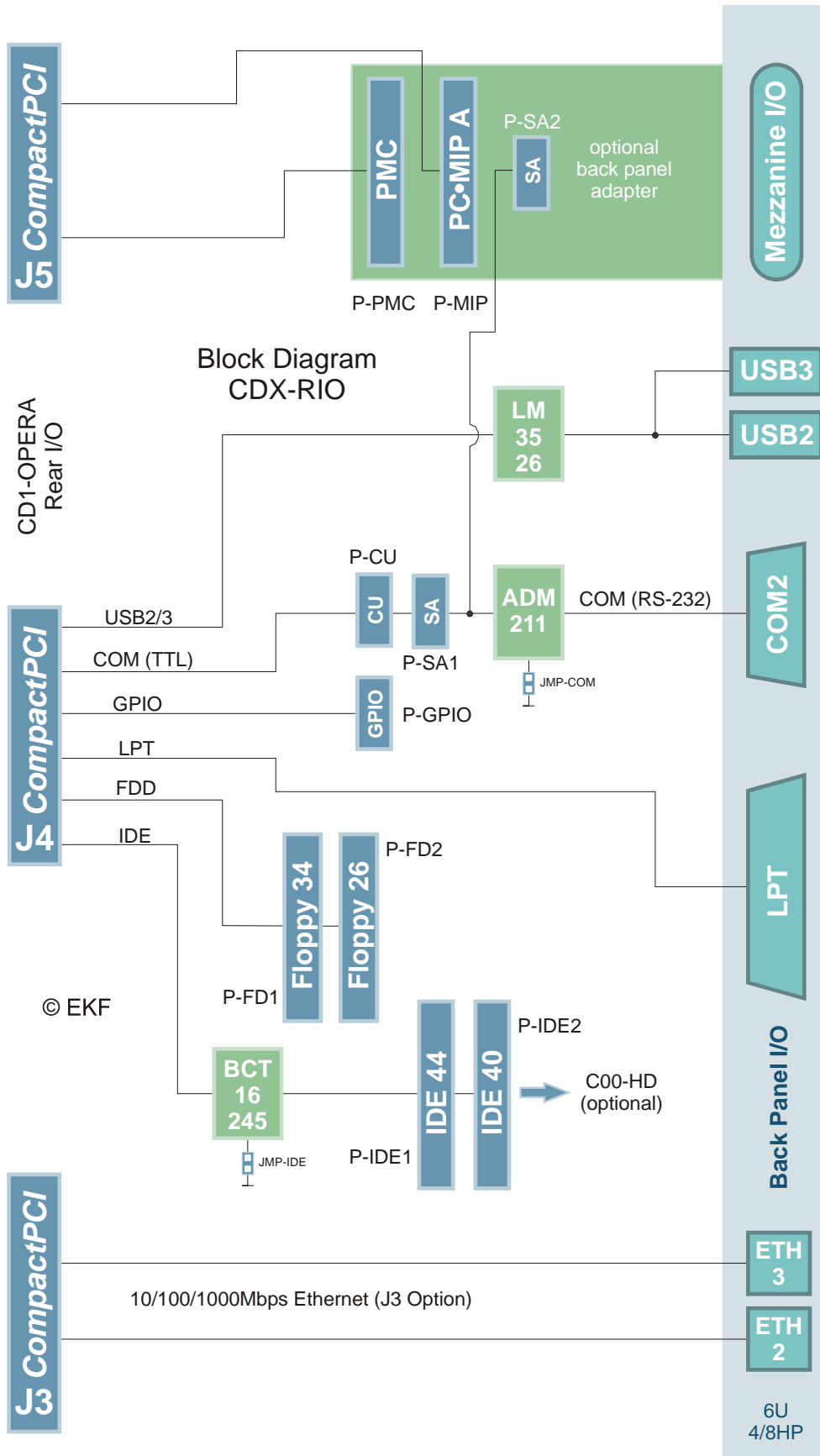


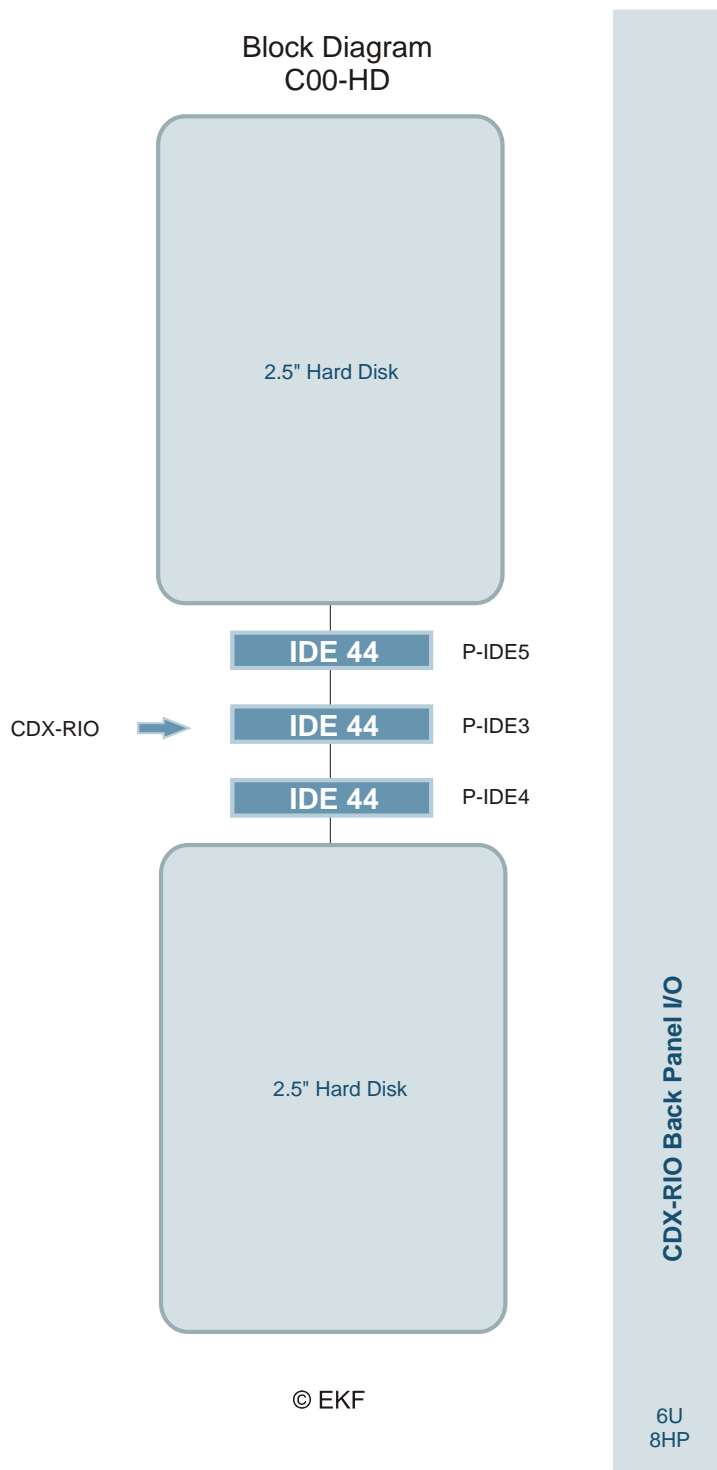
Image CDX-RIO w CD1-OPERA



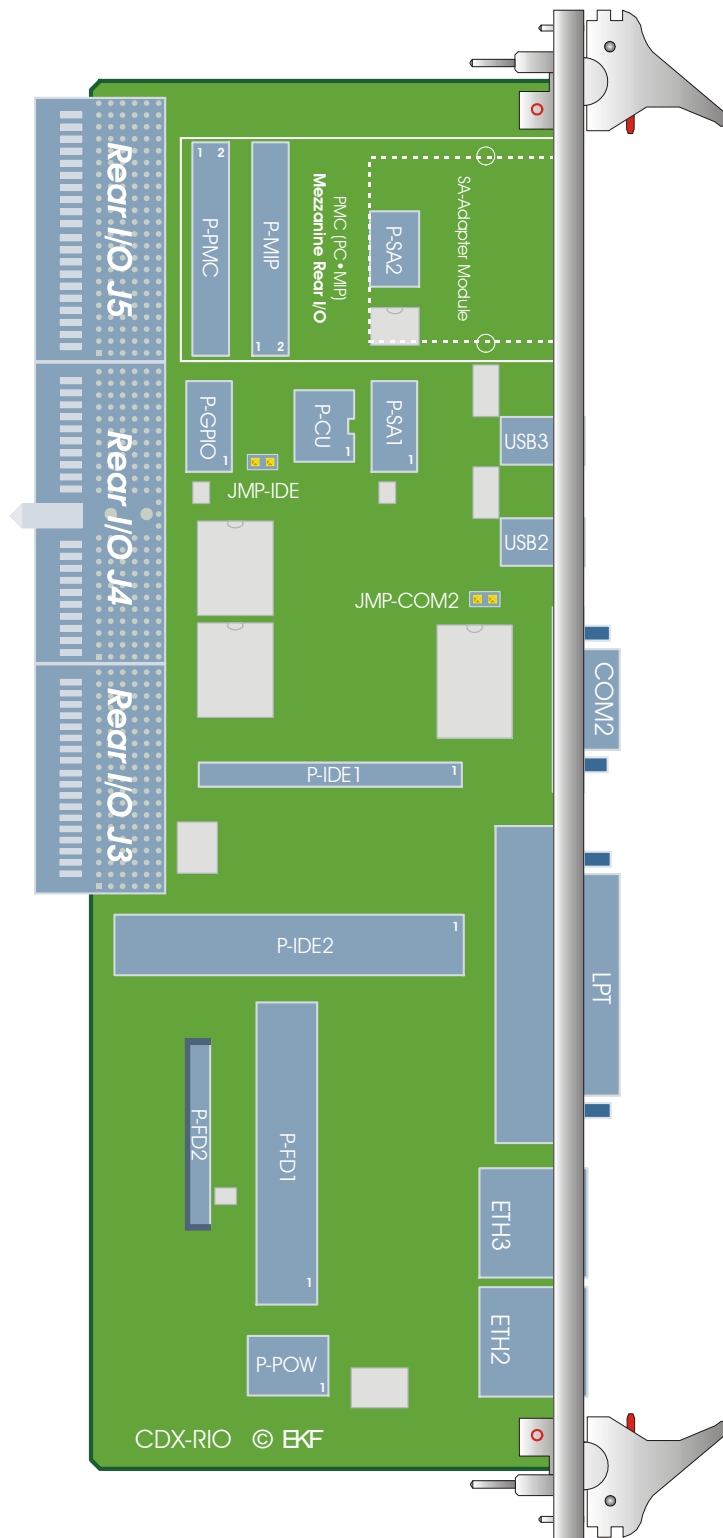
Block Diagram CDX-RIO



Block Diagram C00-HD Option



Top View Component Assembly



## On-Board Connectors

J3	CompactPCI receptacle, matches the CPCI backplane P3 connector <sup>1</sup>
J4	CompactPCI receptacle, matches the CPCI backplane P4 connector
J5	CompactPCI receptacle, matches the CPCI backplane P5 connector <sup>2</sup>
P-CU	Serial interface 10-pin header, suitable for attachment of EKF CU-series PHY modules (e.g. CU7-RS485 and CU8-RS232) <sup>3</sup>
P-FD1	Floppy disk drive 34-pin header, suitable for 3.5" standard floppy disk drives
P-FD2	Floppy disk drive 26-position ZIF socket, suitable for 3.5" micro floppy disk drives
P-GPIO	10-pin GPIO header, for custom specific use
P-IDE1	IDE 44-pin header, suitable for 2.5" hard disk drives, also required for attachment of the hard disk add-on module
P-IDE2	IDE 40-pin header, suitable for 3.5" hard disk drives and DVD drives
P-MIP	IEEE 1386 plug, PMC mezzanine rear I/O, matches the connector 3 on a PC•MIP module <sup>2</sup>
P-PMC	IEEE 1386 receptacle, PMC mezzanine rear I/O, matches the connector 4 on a PMC module <sup>2</sup>
P-POW	Power connector +5V <sup>4</sup>
P-SA1	Serial interface 10-pin header, suitable for attachment of MEN SA-series PHY modules <sup>3</sup>
P-SA2	Serial interface 10-position socket, suitable for plug-in of MEN SA-series PHY modules <sup>3</sup>

<sup>1</sup> J3 is available as an option only. Use of J3, which passes the ETH3 Ethernet connector signals, comes into conflict with the PICMG<sup>®</sup> 2.16 Packet Switching Backplane Specification.

<sup>2</sup> J5 is used to pass over the mezzanine modules rear I/O signals. On your actual CDX-RIO J5 may be left out, as well as the rear I/O mezzanine connectors P-PMC and P-MIP, which carry the signals in the same order as on the CD1-OPERA. When used as a rear panel I/O, an additional back panel adapter module would be required. Please discuss your needs with EKF.

<sup>3</sup> Normally the CDX-RIO is equipped with an on-board RS-232E transceiver and therefore does not require an additional PHY module. As an option, the on-board transceiver can be omitted, and an external PHY module (e.g. isolated RS-485) can be attached.

<sup>4</sup> The CDX-RIO is powered across the J4 connector from the CD1-OPERA. If P-POW is stuffed as an option, the systems +5V power supply may be also connected directly to the CDX-RIO, which may discharge the CD1-OPERA considerably from delivering power especially to the hard disk drives attached to the P-IDE1 connector.

## Back Panel Connectors

COM2	9-pin male D-Sub connector, RS-232E serial interface
ETH2/ETH3	Gigabit Ethernet connector (RJ45) <sup>1</sup>
LPT	25-position female D-Sub connector, parallel printer port
Mezzanine I/O	Normally covered with a bezel, a cutout is provided which is suitable for a custom specific adapter module attached to either connector P-MIP or P-PMC
USB2/USB3	USB type A receptacles, USB 2.0 interfaces

<sup>1</sup> ETH2/ETH3 are provided as an option only. Usage of ETH2/ETH3 comes into conflict with the PICMG<sup>®</sup> 2.16 Packet Switching Backplane Specification. ETH2 is not available with the CD1-OPERA (reserved for future use).

## Installing and Replacing Components

### Before You Begin

#### Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. source and from any telecommunication performing any of the procedures disconnect power, or telecommunication perform any procedures can result in Some parts of the system can continue to operate even though the power switch is in its off state.



Disconnect the system from its power links, networks or modems before described in this chapter. Failure to links before you open the system or personal injury or equipment damage.

#### Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If provide some ESD protection by wearing to a metal part of the system chassis or in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.



such a station is not available, you can an antistatic wrist strap and attaching it board front panel. Store the board only Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

## Installing the Board

### Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighbored front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return



## Removing the Board

### Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only



### Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.





## EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts (e.g. 10Base-2 BNC T-connector)

## Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Isolating Elements	ARP Datacom, 63115 Dietzenbach	Ordering No. 182 068 (Cheapernet T-connector)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

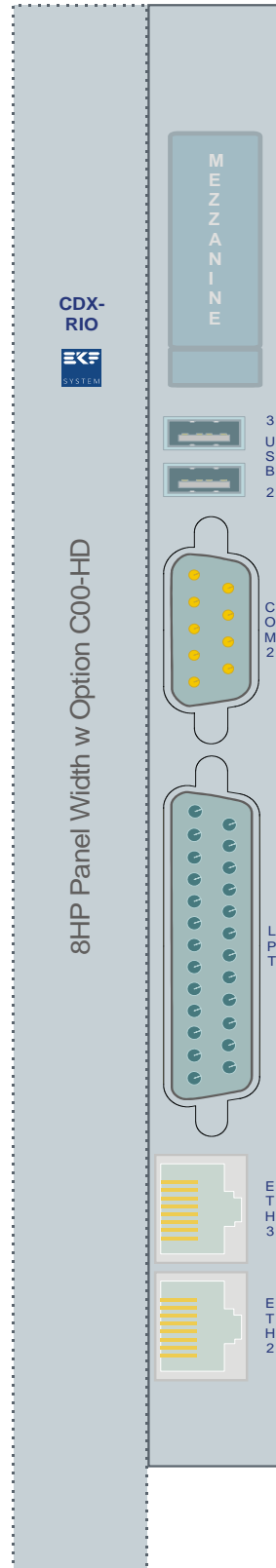
## Technical Reference

### Caution

Some of the connectors may provide operating voltage (e.g. 5V) to devices inside the system chassis, such as internal drives. Not all of these connectors are overcurrent protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

## Back Panel Connectors

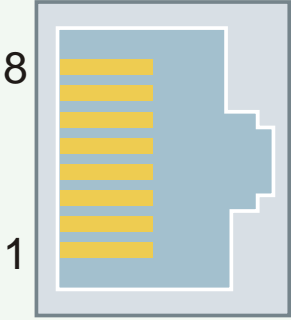
The CDX-RIO is provided with a 6U/4HP (8HP with hard disk add-on module) rear panel, which contains the RJ45 Ethernet jacks, a serial COM port and a parallel printer port D-SUB connector, and two USB receptacles. In addition, a mezzanine rear I/O connector may be mounted into a cutout, which is otherwise covered by a bezel. Characteristic features and the pin assignments of each connector are described on the following pages (connector order from bottom up to top of the back panel).



## ETH2 / ETH3 Ethernet

The CD1-OPERA is equipped with three Gigabit Ethernet controllers. Two of them can be accessed at the front panel, and the third is reserved for either backplane communication or rear I/O.

The ETH3 Ethernet jack is provided as an option only, due to a conflict situation when a Packet Switching Backplane according to PICMG<sup>®</sup> 2.16 is present. That means, if a 2.16 backplane is present in a CompactPCI system, the CPCI connector J3 of the CDX-RIO must be omitted. This measure separates the backplane Ethernet signals from the ETH2/ETH3 jacks. Be sure to discuss your actual needs with sales@ekf.de before ordering the CDX-RIO.

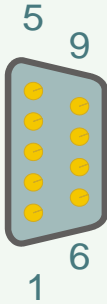


ETH2 & ETH3 (RJ45)		
	1	MDX0+
	2	MDX0-
	3	MDX1+
	4	MDX2+
	5	MDX2-
	6	MDX1-
	7	MDX3+
	8	MDX3-

The ETH2 rear I/O Ethernet jack is not available with the CD1-OPERA (please use the ETH2 jack on the CD1 front panel instead). ETH2 as a rear I/O connector is reserved for future use.

## COM2 Serial Port

The CD1-OPERA CPU board passes over its SIO (Super-I/O) serial interface to the CDX transition module as TTL level signals. Therefore, an on-board RS-232E transceiver is provided (ADM211E).

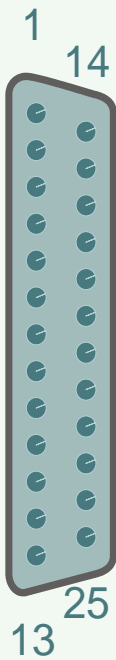
Alternatively, the transceiver may be omitted, and an external PHY module can be attached via either one of the optional on-board headers P-CU (EKF series of CU modules) or P-SA (MEN SA-series). In addition, the transceiver (if stuffed) can also be deactivated by removing the Jumper JMP-COM. If provided, the jumper JMP-COM must be set in order to enable the transceiver and in turn the connector COM2.

COM2 (Male D-Sub 9)				
 <p>JMP-COM</p> <p>removed  COM2 disabled</p> <p>set  COM2 enabled</p>		1	DCD	
	DSR	6		
			2	RXD
	RTS	7		
			3	TXD
	CTS	8		
			4	DTR
	RI	9		
			5	GND

## LPT Parallel Port

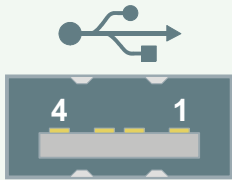
This is a legacy parallel port interface, suitable for attachment of printers (Centronics interface) or for general bidirectional data exchange. The connector is a 25-position female D-Sub, to be used with standard printer cables.

LPT (25-pos. Female D-Sub)				
			13	SLCT
	GND	25		
			12	PE
	GND	24		
			11	BUSY
	GND	23		
			10	ACK#
	GND	22		
			9	D7
	GND	21		
			8	D6
	GND	20		
			7	D5
	GND	19		
			6	D4
	GND	18		
			5	D3
	SLCTIN#	17		
			4	D2
	INIT#	16		
			3	D1
	ERROR#	15		
			2	D0
	ALF#	14		
			1	STROBE#



## USB2 / USB3 High Speed Serial Bus

The rear I/O USB2 & USB3 ports on the CDX transition module are independent from the CD1-OPERA CPU front panel USB interface, thus increasing considerably the overall USB bandwidth available. Each connector can source up to 500mA into external devices and is protected by an electronic switch located on the CDX-RIO board. The interfaces complies to the USB2.0 and USB1.1 specification.

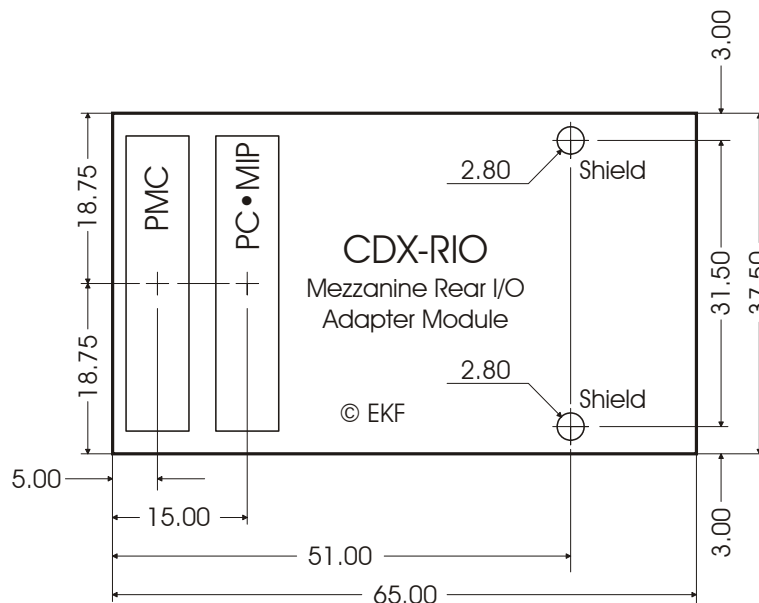
USB2 & USB3		
	1	+5V/0.5A
	2	DATA-
	3	DATA+
	4	GND

## Mezzanine Bezel

The CDX rear panel is provided with a cutout, which is filled with a bezel and a keeper, which in turn is fixed with a screw. The bezel can be deinstalled after removing the keeper. The purpose of the cutout is to accommodate a custom specific I/O connector as part of a mezzanine rear I/O adapter module. This adapter module corresponds to the mezzanine board actually in use on the CD1-OPERA (assuming that the mezzanine module itself makes use of the rear I/O opportunity as specified in the PMC or PC•MIP standards). Hence the mezzanine rear I/O adapter module is a proprietary solution, adjusted to the particular mezzanine module. Simply to say, the mezzanine rear I/O module is a crossover connector board with an IEEE 1386 plug/receptacle on the the inner edge to match either P-PMC or P-MIP, and the I/O connector towards the CDX-RIO back panel. Please contact sales@ekf.de to receive a quote for a mezzanine rear I/O adapter board tailored to your individual needs.

If no mezzanine rear I/O adapter module is present, the vacant space may be used to plug-in a SA-series module onto the socket P-SA2 (serial interface).

Although the bezel mechanics and dimensions comply with the PC•MIP Draft Specification 0.94b chapter 4.6, this solution is in no way restricted to be used with PC•MIP mezzanine boards. It has been chosen due to its small dimensions mainly, and should allow to accommodate a variety of I/O connector types, meaningless if a PMC or PC•MIP mezzanine board is in use.



Dimensions of the Crossover Module (mm)

## On-Board Connectors

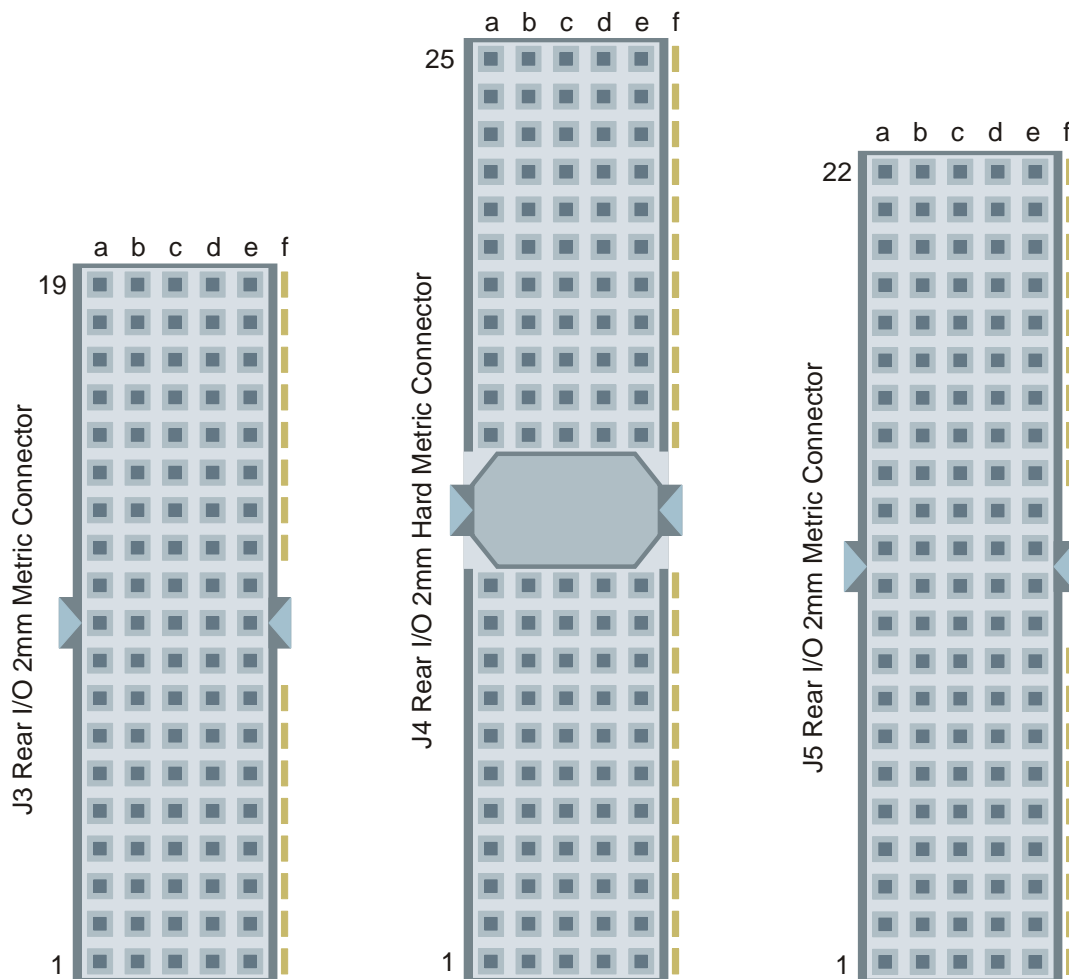
The CDX-RIO transition module may be equipped with several on-board connectors for system internal usage. Not all of these connectors may be present on a particular board. Be sure to specify your individual needs when ordering the CDX board. Characteristic features and the pin assignments of each connector are described on the following pages (connector designation in alphabetical order).

### J3, J4, J5 CompactPCI

J3 is optionally available only, due to a conflict situation when a Packet Switching Backplane according to PICMG® 2.16 is present. J3 is required for passing signals to the ETH2/ETH3 Ethernet jacks.

J4 is stuffed always.

J5 is filled by default, but may be removed if no mezzanine rear I/O facility is needed. J5 is responsible for passing signals to the P-PMC and P-MIP IEEE 1386 connectors.



Column f is used for shielding

#J3	A	B	C	D	E
19	GND	GND	GND	GND	GND
18	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-
17	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-
16	NC LPb_DA+	NC LPb_DA-	GND	NC LPb_DC+	NC LPb_DC-
15	NC LPb_DB+	NC LPb_DB-	GND	NC LPb_DD+	NC LPb_DD-
14	GND	GND	GND	GND	GND
13	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
10	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC
8	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC
6	NC	NC	NC	NC	NC
5	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC
3	NC	NC	NC	NC	NC
2	NC	NC	NC	NC	NC
1	NC	NC	NC	NC	NC

LPa\_xxx -> ETH3

LPb\_xxx -> ETH2

#J4	A	B	C	D	E
25	NC	GPIO8	GPIO12	NC	USB P2+
24	NC	GPIO9	GPIO13	NC	USB P2-
23	NC	GPIO10	GPIO14	NC	USB P1+
22	COM2 RI#	GPIO11	GPIO15	+5V	USB P1-
21	COM2 RTS#	COM2 DSR#	COM2 CTS#	COM2 DCD#	USB OC#
20	NC	+5V	COM2 TXD	COM2 RXD	COM2 DTR#
19	GND	GND	NC	NC	NC
18	LPT PE	LPT SLCT	+5V	GND	NC
17	LPT D05	LPT D06	LPT D07	LPT ACK#	LPT BUSY
16	LPT INIT#	LPT D02	LPT SLCTIN#	LPT D03	LPT D04
15	LPT STROBE#	LPT ALF#	LPT D00	LPT ERROR#	LPT D01
14					
13	KEY AREA				
12					
11	FDD TRK0#	FDD WRTprt#	FDD RDATA#	FDD HDSEL#	FDD DSKCHG#
10	GND	FDD DIR#	FDD STEP#	FDD WDATA#	FDD WGATE#
9	FDD DRVDEN0#	FDD INDEX#	FDD MTR0#	GND	FDD DS0#
8	+5V	GND	NC +12V	GND	NC +12V
7	+5V	IDE CS1#	GND	IDE CS3#	IDE ACT#
6	IDE DACK#	IDE IRQ14	IDE A01	IDE A00	IDE A02
5	GND	IDE IOW#	GND	IDE IOR#	IDE IORDY
4	IDE D14	IDE D00	IDE D15	GND	IDE DREQ
3	IDE D03	IDE D12	IDE D02	IDE D13	IDE D01
2	IDE D09	IDE D05	IDE D10	IDE D04	IDE D11
1	IDE RST#	GND	IDE D07	IDE D08	IDE D06

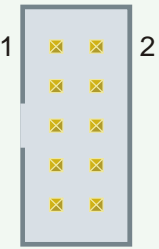
#J5	A	B	C	D	E
22	PCMIP64	PCMIP63	PCMIP62	PCMIP61	PCMIP60
21	PCMIP59	PCMIP57	PCMIP56	PCMIP55	PCMIP54
20	PCMIP52	PCMIP51	PCMIP49	PCMIP48	PCMIP47
19	PCMIP46	PCMIP44	PCMIP43	PCMIP41	PCMIP40
18	PCMIP39	PCMIP38	PCMIP36	PCMIP35	PCMIP33
17	PCMIP32	PCMIP31	PCMIP30	PCMIP28	PCMIP27
16	PCMIP25	PCMIP24	PCMIP23	PCMIP22	PCMIP20
15	PCMIP19	PCMIP17/PMC1	PCMIP16/PMC2	PCMIP15/PMC3	PCMIP14/PMC4
14	PCMIP12/PMC5	PCMIP11/PMC6	PCMIP9/PMC7	PCMIP8/PMC8	PCMIP7/PMC9
13	PCMIP6/PMC10	PCMIP4/PMC11	PCMIP3/PMC12	PCMIP2/PMC13	PCMIP1/PMC14
12	+3.3V	+3.3V	+3.3V	+5V	+5V
11	PMC15	PMC16	PMC17	PMC18	PMC19
10	PMC20	PMC21	PMC22	PMC23	PMC24
9	PMC25	PMC26	PMC27	PMC28	PMC29
8	PMC30	PMC31	PMC32	PMC33	PMC34
7	PMC35	PMC36	PMC37	PMC38	PMC39
6	PMC40	PMC41	PMC42	PMC43	PMC44
5	PMC45	PMC46	PMC47	PMC48	PMC49
4	PMC50	PMC51	PMC52	PMC53	PMC54
3	PMC55	PMC56	PMC57	PMC58	PMC59
2	PMC60	PMC61	PMC62	PMC63	PMC64
1	+3.3V	+3.3V	+3.3V	+5V	+5V

### P-CU Serial Interface Connectors

If the on-board RS-232 transceiver ADM211E is either not stuffed or disabled by removing the jumper JMP-COM, alternatively external PHY modules can be attached to the CDX-RIO by means of a flat ribbon cable.

The rear I/O transition module is equipped with the header P-CU, suitable for the EKF CU7/CU8 series of PHY modules. The CU7-RS485 is an isolated fieldbus interface, available either for party-line configuration or full-duplex point-to-point.

Another pair of headers P-SA1/2 may be provided on the CDX-RIO which complies with the MEN SA-series of PHY modules. No more than one transceiver may be in use, either P-CU, P-SA or the on-board transceiver.

P-CU (2.00mm Pin Header 2 x 5)				
 <p>2.00mm Pin Header</p>	+5V/0.5A	1	2	DSR#
	RI#	3	4	RXD
	TXD	5	6	DTR#
	RTS#	7	8	CTS#
	DCD#	9	10	GND

### JMP-COM



Remove JMP-COM to disable the on-board transceiver when using P-CU

## P-FD1 Floppy Disk Drive

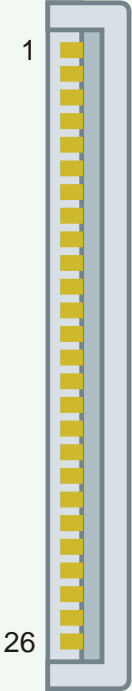
The CDX-RIO is provided with a 34-pin header, suitable for attachment of a single floppy disk drive with mating connector.

P-FD1 (2.54mm Header)				
	GND	1	2	drvden0#
	GND	3	4	NC
	KEY	5	6	NC
	GND	7	8	index#
	GND	9	10	mtr0#
	GND	11	12	NC
	GND	13	14	ds0#
	GND	15	16	NC
	GND	17	18	dir#
	GND	19	20	step#
	GND	21	22	wdata#
	GND	23	24	wgate#
	GND	25	26	trk0#
	GND	27	28	wrtprt#
	NC	29	30	rdata#
	GND	31	32	hdsel#
	NC	33	34	dskchg#

## P-FD2 Floppy Disk Drive

In addition to P-FD1, the CDX-RIO is also provided with a 26-position FFC/FPC ZIF socket, suitable for attachment of a single floppy disk drive with mating connector (typically low profile drives, e.g. TEAC FD05HF5630, Y-E Data YD-702J-6637, Citizen X1DE-00R, Mitsumi D353F3, Samsung SFD-321S, NEC FD1238H).

You may chose either the P-FD2 connector or P-FD1, but not both simultaneously.

P-FD1 (FFC/FPC 1mm ZIF Receptacle)		
 <p>1mm pitch FFC/FPC receptacle vertikal ZIF 26-position</p>	1	+5V
	2	index#
	3	+5V
	4	ds0#
	5	+5V
	6	dskchg#
	7	NC
	8	NC
	9	drvden0#
	10	mtr0#
	11	NC
	12	dir#
	13	modsel
	14	step#
	15	GND
	16	wdata#
	17	GND
	18	wgate#
	19	GND
	20	trk0#
	21	NC
	22	wrtprt#
	23	GND
	24	rdata#
	25	GND
	26	hdsel#

### P-IDE1 IDE

The optional CDX transition module on-board connector P-IDE1 is a dual row 2 x 22 pin header (2.00mm pitch), suitable for attachment of up to two 2.5-inch hard disk drives, configured as master and slave devices attached to a common flat ribbon cable. Both connectors P-IDE2 and P-IDE1 are assigned to the primary IDE interface of the CD1 CPU board. Because no branches or open endings are allowed on the IDE bus, only a single connector, either P-IDE2 or P-IDE1 may be in use. P-IDE2/P-IDE1 can be deactivated by means of analog switches provided on the CDX transition module as described in the chapter "P-IDE2 IDE/ATA" of this manual.

The metric connector P-IDE1 matches the typical 2.5-inch hard disk drive connector. Suitable 1.00mm pitch flat ribbon cable assemblies are available from EKF. Drive power is also delivered to P-IDE1. If drive power is sourced by the CD1-OPERA across J4, the maximum power consumption of the attached IDE device(s) should be less than ~3W. Therefore, consider the usage of a discrete power strap from the systems supply to the connector P-POW on the CDX-RIO.

P-IDE1 (2.00mm Header)				
	reset#	1	2	GND
	d07	3	4	d08
	d06	5	6	d09
	d05	7	8	d10
	d04	9	10	d11
	d03	11	12	d12
	d02	13	14	d13
	d01	15	16	d14
	d00	17	18	d15
	GND	19	20	KEY
	dmarq	21	22	GND
	iow#	23	24	GND
	ior#	25	26	GND
	iordy	27	28	GND
	dmack#	29	30	GND
	intrq	31	32	NC
	a1	33	34	NC
	a0	35	36	a2
	cs1#	37	38	cs3#
	act#	39	40	GND
	drvpwr	41	42	drvpwr
	GND	43	44	NC

**JMP-IDE**

removed IDE disabled

set IDE enabled

## P-IDE2 IDE/ATA

The optional on-board connector P-IDE2 is a dual row 2 x 20 pin header (2.54mm pitch), suitable for attachment of up to two 3.5-inch hard disks and/or CD-ROM or DVD drives, configured as master and slave devices attached to a common flat ribbon cable (use special 80-pin cabling assembly for Ultra ATA/66 and Ultra ATA/100 operation). P-IDE2 is the primary IDE port of the CD1-OPERA.

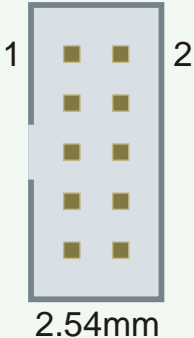
Routing of IDE signals is extremely critical. No branches or open endings are allowed on the IDE bus. Therefore, either one of the rear I/O headers P-IDE2/P-IDE1 may be in use, but never both connectors simultaneously. The CDX is also provided with analog switches, which allow to cut off the IDE bus close to the CompactPCI connector J4, in order to reduce signal reflections if neither P-IDE2 nor P-IDE1 are in use. By default, the switches are set to 'on' (pass through). The switches can be disabled by removing the jumper JMP-IDE (if provided). As an alternative stuffing option, the GPIO15 line is used to enable/disable the IDE switches on the CDX transition module. Check the CD1 BIOS setup for the appropriate settings.

P-IDE2 (2.54mm Shrouded Header)				
	reset#	1	2	GND
	d07	3	4	d08
	d06	5	6	d09
	d05	7	8	d10
	d04	9	10	d11
	d03	11	12	d12
	d02	13	14	d13
	d01	15	16	d14
	d00	17	18	d15
	GND	19	20	KEY
	dmarq	21	22	GND
	iow#	23	24	GND
	ior#	25	26	GND
	iordy	27	28	GND
	dmack#	29	30	GND
	intrq	31	32	NC
	a1	33	34	NC
	a0	35	36	a2
	cs1#	37	38	cs3#
	act#	39	40	GND

### P-GPIO Connector

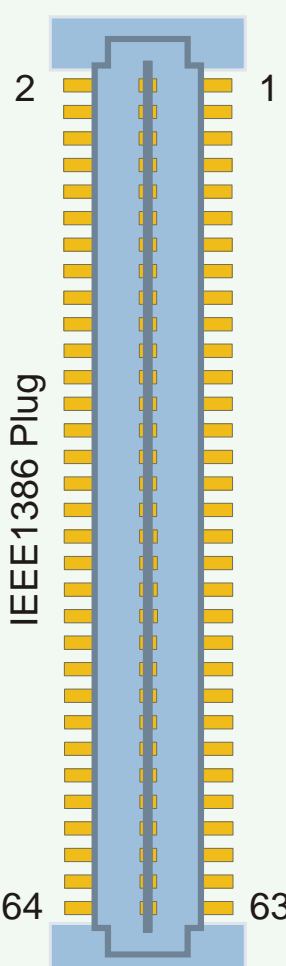
The CD1-OPERA CPU board may be provided with a PLD chip (Altera EP1K30), which makes available several general purpose input/output signals. A group of 8 GPIOs are passed through to the CDX rear I/O transition module connector GPIO (optional), dual row 2 x 5, 2.54mm pin header. The GPIO lines are TTL (8mA sink as an output) or CMOS compatible, 3.3V logic (inputs are 5V tolerant). The behaviour of each particular line can be programmed.

As of current, the P-GPIO feature is not yet available. Please contact [sales@ekf.de](mailto:sales@ekf.de) to discuss your specific needs.

P-GPIO (2.54mm Header 2 x 5)				
	GND	1	2	+5V/0.5A
	GPIO8	3	4	GPIO9
	GPIO10	5	6	GPIO11
	GPIO12	7	8	GPIO13
	GPIO14	9	10	GPIO15 <sup>1</sup>

<sup>1</sup> In certain configurations of the CDX-RIO, GPIO15 may also be used to enable/disable the IDE connectors by means of the BIOS settings of the CD1-OPERA.

## P-MIP Mezzanine Connector

P-MIP				
	MAJ3 (PCMIP) 2	2	1	MAJ3 (PCMIP) 1
	MAJ3 (PCMIP) 4	4	3	MAJ3 (PCMIP) 3
	MAJ3 (PCMIP) 6	6	5	GND
	MAJ3 (PCMIP) 8	8	7	MAJ3 (PCMIP) 7
	GND	10	9	MAJ3 (PCMIP) 9
	MAJ3 (PCMIP) 12	12	11	MAJ3 (PCMIP) 11
	MAJ3 (PCMIP) 14	14	13	GND
	MAJ3 (PCMIP) 16	16	15	MAJ3 (PCMIP) 15
	GND	18	17	MAJ3 (PCMIP) 17
	MAJ3 (PCMIP) 20	20	19	MAJ3 (PCMIP) 19
	MAJ3 (PCMIP) 22	22	21	GND
	MAJ3 (PCMIP) 24	24	23	MAJ3 (PCMIP) 23
	GND	26	25	MAJ3 (PCMIP) 25
	MAJ3 (PCMIP) 28	28	27	MAJ3 (PCMIP) 27
	MAJ3 (PCMIP) 30	30	29	GND
	MAJ3 (PCMIP) 32	32	31	MAJ3 (PCMIP) 31
	GND	34	33	MAJ3 (PCMIP) 33
	MAJ3 (PCMIP) 36	36	35	MAJ3 (PCMIP) 35
	MAJ3 (PCMIP) 38	38	37	GND
	MAJ3 (PCMIP) 40	40	39	MAJ3 (PCMIP) 39
	GND	42	41	MAJ3 (PCMIP) 41
	MAJ3 (PCMIP) 44	44	43	MAJ3 (PCMIP) 43
	MAJ3 (PCMIP) 46	46	45	GND
	MAJ3 (PCMIP) 48	48	47	MAJ3 (PCMIP) 47
	GND	50	49	MAJ3 (PCMIP) 49
	MAJ3 (PCMIP) 52	52	51	MAJ3 (PCMIP) 51
	MAJ3 (PCMIP) 54	54	53	GND
	MAJ3 (PCMIP) 56	56	55	MAJ3 (PCMIP) 55
	GND	58	57	MAJ3 (PCMIP) 57
	MAJ3 (PCMIP) 60	60	59	MAJ3 (PCMIP) 59
	MAJ3 (PCMIP) 62	62	61	MAJ3 (PCMIP) 61
	MAJ3 (PCMIP) 64	64	63	MAJ3 (PCMIP) 63

If a PC•MIP mezzanine module is present on the mezzanine module slot A of the CD1-OPERA, then this modules rear I/O lines are passed across J5 of the CDX-RIO to the connector P-MIP (IEEE 1386 plug). A crossover mezzanine rear I/O adapter module would be needed in addition, aligned towards the cutout covered normally by the bezel, in order to provide access from the rear panel. Because each PC•MIP module may have its own signal order on the rear I/O channel, and due to a variety of rear panel connector types, the mezzanine adapter module also must be individually designed to meet the specifications of the particular PC•MIP in use. Please contact [sales@ekf.de](mailto:sales@ekf.de) for a quote.

P-PMC Mezzanine Connector


P-PMC				
	MDJ4 (PMC) 1	1	2	MDJ4 (PMC) 2
	MDJ4 (PMC) 3	3	4	MDJ4 (PMC) 4
	MDJ4 (PMC) 5	5	6	MDJ4 (PMC) 6
	MDJ4 (PMC) 7	7	8	MDJ4 (PMC) 8
	MDJ4 (PMC) 9	9	10	MDJ4 (PMC) 10
	MDJ4 (PMC) 11	11	12	MDJ4 (PMC) 12
	MDJ4 (PMC) 13	13	14	MDJ4 (PMC) 14
	MDJ4 (PMC) 15	15	16	MDJ4 (PMC) 16
	MDJ4 (PMC) 17	17	18	MDJ4 (PMC) 18
	MDJ4 (PMC) 19	19	20	MDJ4 (PMC) 20
	MDJ4 (PMC) 21	21	22	MDJ4 (PMC) 22
	MDJ4 (PMC) 23	23	24	MDJ4 (PMC) 24
	MDJ4 (PMC) 25	25	26	MDJ4 (PMC) 26
	MDJ4 (PMC) 27	27	28	MDJ4 (PMC) 28
	MDJ4 (PMC) 29	29	30	MDJ4 (PMC) 30
	MDJ4 (PMC) 31	31	32	MDJ4 (PMC) 32
	MDJ4 (PMC) 33	33	34	MDJ4 (PMC) 34
	MDJ4 (PMC) 35	35	36	MDJ4 (PMC) 36
	MDJ4 (PMC) 37	37	38	MDJ4 (PMC) 38
	MDJ4 (PMC) 39	39	40	MDJ4 (PMC) 40
	MDJ4 (PMC) 41	41	42	MDJ4 (PMC) 42
	MDJ4 (PMC) 43	43	44	MDJ4 (PMC) 44
	MDJ4 (PMC) 45	45	46	MDJ4 (PMC) 46
	MDJ4 (PMC) 47	47	48	MDJ4 (PMC) 48
	MDJ4 (PMC) 49	49	50	MDJ4 (PMC) 50
	MDJ4 (PMC) 51	51	52	MDJ4 (PMC) 52
	MDJ4 (PMC) 53	53	54	MDJ4 (PMC) 54
	MDJ4 (PMC) 55	55	56	MDJ4 (PMC) 56
	MDJ4 (PMC) 57	57	58	MDJ4 (PMC) 58
	MDJ4 (PMC) 59	59	60	MDJ4 (PMC) 60
	MDJ4 (PMC) 61	61	62	MDJ4 (PMC) 62
	MDJ4 (PMC) 63	63	64	MDJ4 (PMC) 64

If a PMC mezzanine module is present on the CD1-OPERA (mezzanine module slot D), then this modules rear I/O lines are passed across J5 of the CDX-RIO to the connector P-PMC (IEEE 1386 receptacle). A crossover mezzanine rear I/O adapter module would be needed in addition, aligned with its I/O connector protruding through the cutout covered normally by the bezel, thus providing access from the rear panel. Because each PMC module may have its own signal order on the rear I/O channel, and due to a variety of rear panel connector types, the mezzanine adapter module also must be individually designed to meet the specifications of the particular PMC in use. Please contact sales@ekf.de for a quote.

### Power Connector P-POW

The CDX rear I/O transition module can be supplied with +5V across the J4/J5 connectors from the CD1-OPERA CPU board. +5V would be required for the CDX on-board RS-232E transceiver, and for IDE devices possibly attached to the 44-lead connector P-IDE1, which passes directly power to the drive(s).

With the optional connector P-POW, the systems power supply can be directly connected to the CDX-RIO transition module, discharging the CD1-OPERA up to a maximum of 2.5A @5V. The connector is an AMP EI series 4-position header (#171826-4), being very popular since it is used also on 3.5-inch floppy disk drives. The current is limited by a resettable fuse.

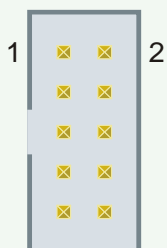
P-POW		
 <p>AMP 171826-4</p>	1	+5V/2.5A
	2	GND
	3	GND
	4	NC

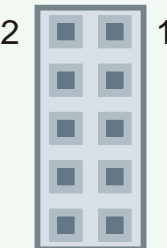
### P-SA1 / P-SA2 Serial Interface Connectors

If the on-board RS-232 transceiver ADM211E is either not stuffed or disabled by removing the jumper JMP-COM, alternatively external PHY modules can be attached to the CDX-RIO by means of a flat ribbon cable.

The rear I/O transition module may be equipped with the header P-SA1 and/or socket P-SA2, suitable for the MEN SA-series of PHY modules. P-SA2 would allow to plug the SA-module directly onto the CDX-RIO, if no mezzanine rear I/O adapter module is present.

Another header P-CU may be provided on the CDX-RIO which complies with the EKF CU-series of PHY modules. No more than one transceiver may be in use, either P-CU, P-SAx or the on-board transceiver.

P-SA1 (2.54mm Pin Header 2 x 5)				
 <p>2.54mm Plug</p>	GND	1	2	+5V/0.5A
	TXD	3	4	RXD
	DTR#	5	6	RTS#
	DSR#	7	8	CTS#
	DCD#	9	10	RI#

P-SA2 (2.54mm Socket 2 x 5)				
 <p>2.54mm Socket</p>	+5V/0.5A	2	1	GND
	RXD	4	3	TXD
	RTS#	6	5	DTR#
	CTS#	8	7	DSR#
	RI#	10	9	DCD#

#### JMP-COM

removed  COM2 disabled

set  COM2 enabled

Remove JMP-COM to disable the on-board transceiver when using P-SAx

## Schematics

Complete circuit diagrams for this product are available for customers on request. Signing of a non-disclosure agreement would be needed. Please contact [sales@ekf.de](mailto:sales@ekf.de) for details.

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